# GANDHI SCHOOL OF ENGINEERING

## BHABANDHA,BERHAMPUR

## PROPOSED WORK

## 3rd SEM SUBJECT- Th.3 - DIGITAL ELECTRONICS

## NAME OF FACULTY- PRABHAMAYEE ACHARYA

| SL NO. CHAPTER | TOPICS | NO OF PERIODS ASSIGNED BY SCTE&VT | PLANNING DATES | REMARKS |
|---|---|---|---|---|
| 1 | **Basics of Digital Electronics**<br>1.1 Number System-Binary, Octal, Decimal, Hexadecimal - Conversion from one system to another number system.<br>1.2 Arithmetic Operation-Addition, Subtraction, Multiplication, Division, 1's & 2's complement of Binary numbers& Subtraction using complements method<br>1.3 Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes, excess-3 and Gray codes.<br>1.4 Logic gates: AND,OR,NOT,NAND,NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagram<br>1.5 Universal Gates& its Realisation<br>1.6 Boolean algebra, Boolean expressions, Demorgan's Theorems.<br>1.7 Represent Logic Expression: SOP & POS forms<br>1.8 Karnaugh map (3 & 4 | 12 | 01 OCT 2021<br>To<br>02 N0V 2021 | |

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| | Variables)&Minimization of logical expressions ,don't care conditions | | | |
| 2 | **Combinational logic circuits** <br> 2.1 Half adder, Full adder, Half Subtractor, Full Subtractor, Serial and Parallel Binary 4 bit adder. <br> 2.2 Multiplexer (4:1), De- multiplexer (1:4), Decoder, Encoder, Digital comparator (3 Bit) <br> 2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit, truth table, Applications of above | 12 | **03 NOV 2021** <br> **To** <br> **24 NOV 2021** | |
| 3 | **Sequential logic Circuits** <br> 3.1 Principle of flip-flops operation, its Types, <br> 3.2 SR Flip Flop using NAND,NOR Latch (un clocked) <br> 3.3 C l o c k e d SR,D,JK,T,JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications <br> 3.4 Concept of Racing and how it can be avoided. | 12 | **25 NOV 2021** <br> **To** <br> **14 DEC 2021** | |
| 4 | **Registers, Memories & PLD** <br> 4.1 Shift Registers-Serial in Serial -out, Serial- in Parallel-out, Parallel in serial out and Parallel in parallel out <br> 4.2 Universal shift registers-Applications. <br> 4.3 Types of Counter & applications <br> 4.4 Binary counter, Asynchronous ripple counter (UP & DOWN), Decade counter. Synchronous counter, Ring Counter. <br> 4.5 Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM <br> 4.6 Basic concept of PLD & applications | 08 | **15 DEC 2021** <br> **To** <br> **27 DEC 2021** | |

| 5 | **A/D and D/A Converters**<br>5.1 Necessity of A/D and D/A converters.<br>5.2 D/A conversion using weighted resistors methods.<br> 5.3 D/A conversion using R-2R ladder (Weighted resistors) network.<br>5.4 A/D conversion using counter method.<br>5.5 A/D conversion using Successive approximate method | 07 | **28 DEC 2021<br>To<br>03 JAN 2022** | |
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| 6 | **LOGIC FAMILIES**<br>6.1 Various logic families &categories according to the IC fabrication process<br>6.2 Characteristics of Digital ICs- Propagation Delay, fan-out, fan-in, Power Dissipation ,Noise Margin ,Power Supply requirement &Speed with Reference to logic families.<br> 6.3 Features, circuit operation &various applications of TTL(NAND), CMOS (NAND & NOR) | 09 | **04 JAN 2022<br>To<br>17 JAN 2022** | |

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